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May 1974

NIC # 19716
Packet Radio Temporary Note 79

Equalizers for PRN

ABSTRACT

Equalizers have been extensively studied and successfully implemented for telephone and television channels. Here the basic principles and components of equalizers are reviewed. The classification of equalizers is considered. The hardware realizations and schematic diagrams of several existing schemes are described in detail. These schemes are compared as regards principle, type, complexity, and hardware elements. The packet radio issues are described. The extension of equalizers to PRN is not direct because of the vast difference in requirements. Two hypothetical situations are analyzed. The problem is to be further looked into when the PR issues have been well defined.

I Introduction

Equalizers have been extensively studied with reference to telephone channels. At present, economical, efficiently built, and reliable equalizers are available up to data rates of 9600 b/s. In recent years, an adaptive equalizer has been successfully implemented for television channels. It has been suggested[1] that equalizers be used for packet radio (PR) to improve performance. Theoretically, the problem appears to be simple extension, but as summarized in Table 1, there are distinct differences among the above applications.

Since the characteristics vary so widely, the hardware requirements in terms of speed differ. Hence this study is undertaken to examine the situation critically and to explore the possibilities and feasibility of using equalizers for PRN.

Table 1

SUMMARY OF CHANNEL CHARACTERISTICS

System Parameter	Telephone	Television	PRN*
Bandwidth	3 kHz	4.6 MHz	40 MHz
Bit rate	9.6 kb/s	Picture	100 kb/s
Type	Digital/analog	Analog	Digital
Mode of transmission	DDD/Private Line	VHF	ALOHA (random access)
Modulation	PSK/FSK	Analog	Spread spectrum
Number of amplitude levels	Multilevel	--	Preferably two
Nature of distortion	Intersymbol interference	Delay and amplitude	Multipath

* NOTE: These are existing characteristics. They are likely to change.

A vast literature exists in the field of equalizers.[2-21] This note summarizes the main concepts needed for understanding of the basic principles. The background material is explained in terms of the function of each of the components. The classifications of equalizers is considered. The existing schemes are briefly described, to indicate the hardware needed, and are compared in terms of typical parameters, such as complexity.

The PR issues are examined in detail. Since many of the characteristics are not well known at this time, a hypothetical situation similar to PR is thoroughly analyzed to give an idea of the hardware necessary for a typical equalizer. When these characteristics have been well defined for PRN, further investigation into the need for equalizers will be required, since with the present characteristics there appears to be no need for them.

II Background

Recently, tremendous effort has been devoted to achieving greater transmission efficiencies from already crowded channels. The effort has been successful in the areas of error control schemes and signal design. An obstacle for efficient transmission is residual dispersion or linear distortion. Such distortion manifests in two ways: In wire communications it is called linear distortion or intersymbol interference, and in radio communications it is called multipath. The problems resulting from linear distortion or multipath are similar, except that multipath is often a time-varying phenomenon. The equalizer is used to minimize the distortion introduced in the channel.

The distortion in the channel occurs mainly in the form of amplitude and phase variations of channel response. These variations are caused by:

(1) Time spread of response.

(2) Frequency spread of response because of Doppler, time jitter, or time-variable frequency offset.

(3) Low-level added Gaussian noise of slowly varying rms value.

(4) High-level interference bursts from impulse noise or common channel interference.

(5) Nonlinearity arising from transmitter-overdrive receiver saturation.

Item (4) is usually solved by using burst-error-correcting codes; the main imparments are caused by Items (1) and (2).

III Principle of Equalizer Use

Intensive efforts have been made to take care of channel distortion problems by equalization. The general scheme used to achieve equalization is depicted as a block diagram in Figure 1. Figure 2 shows a more detailed structure of a simple, conventional equalizer.

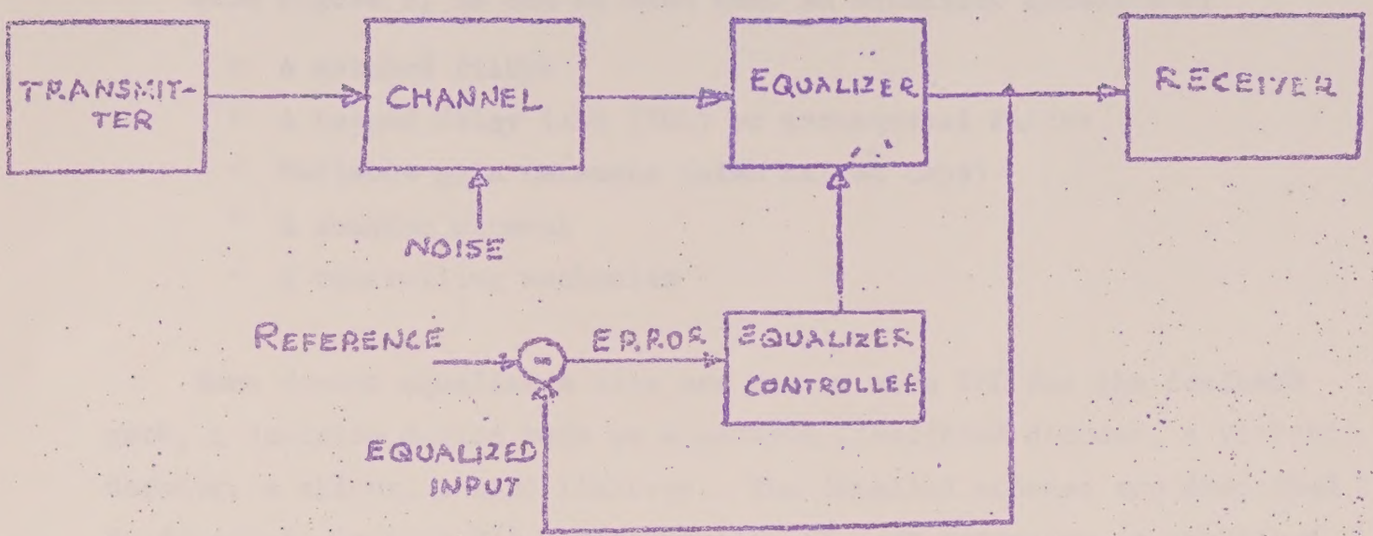
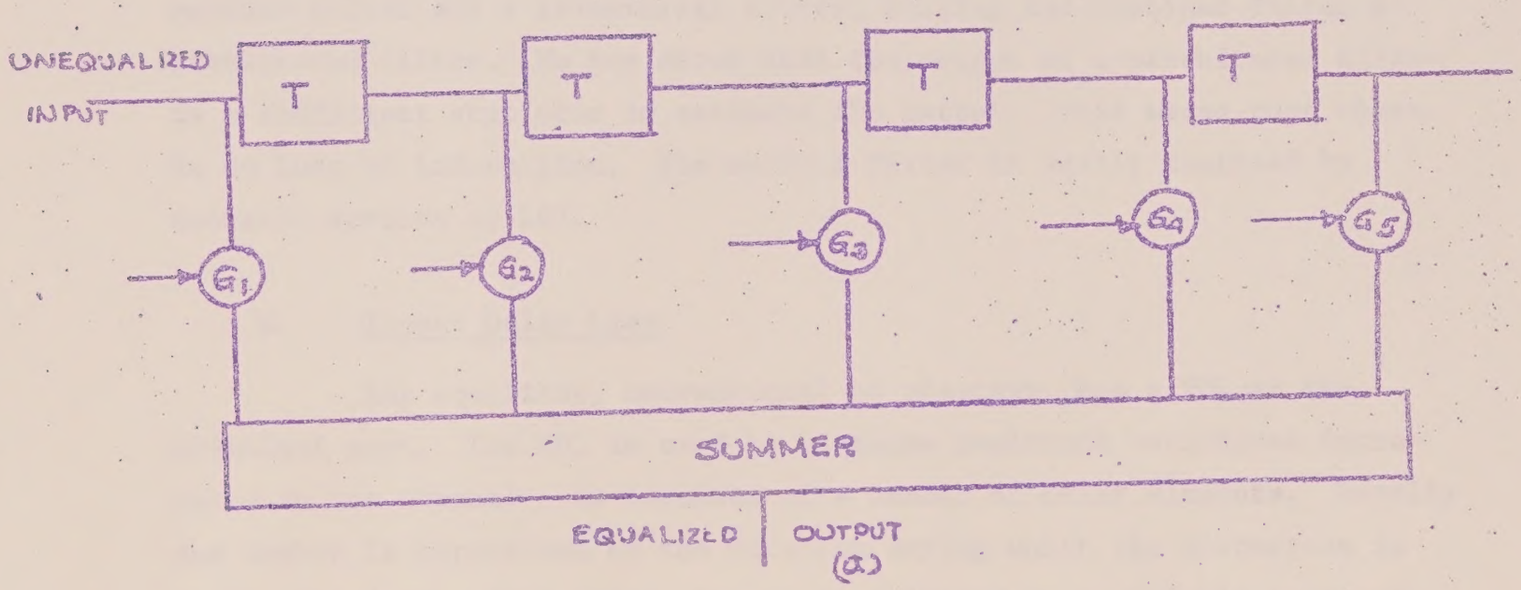


FIG. 1. THE COMMUNICATION SYSTEM WITH EQUALIZER



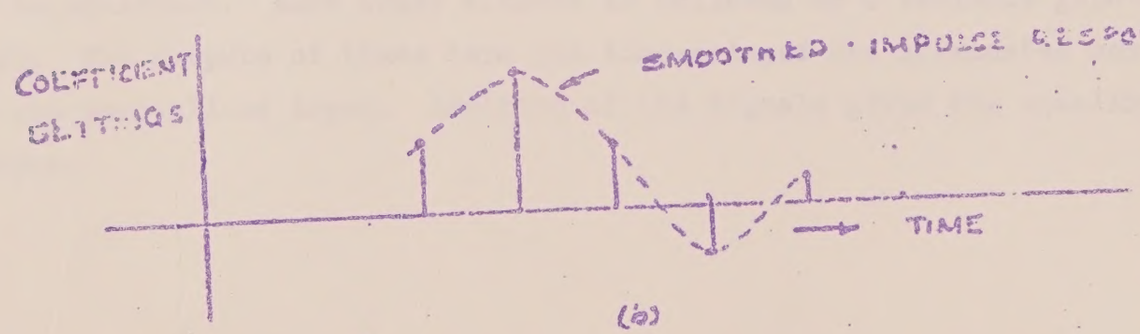
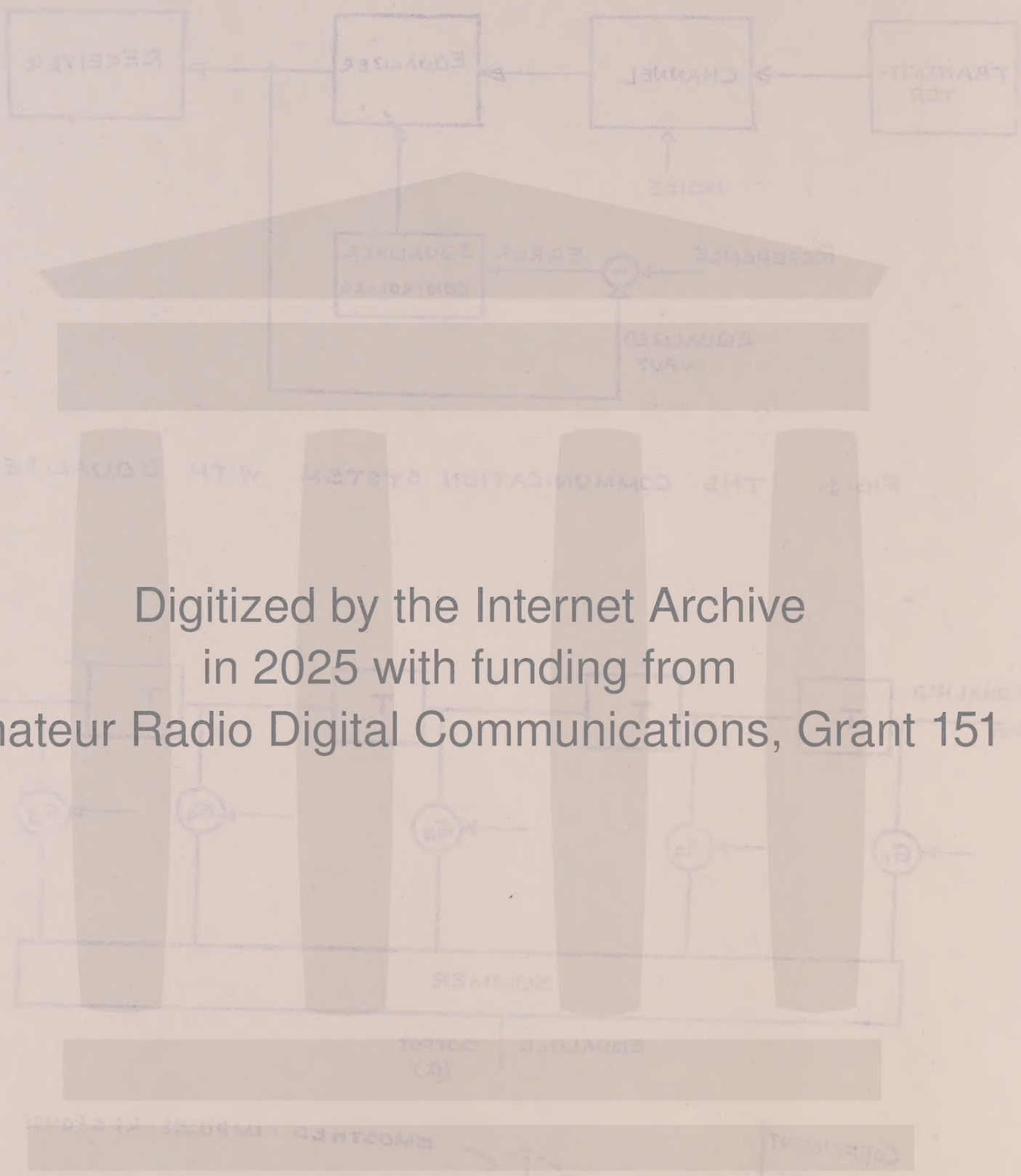


FIG 2. (a) DETAILED STRUCTURE OF EQUALIZER b) IMPULSE RESPONSE
BY SUITABLY ALTERING IMPULSE RESPONSE THE ZEROS CAN BE FORCED ANYWHERE



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From Figure 2, it can be seen that an equalizer consists of

- A matched filter
- A tapped delay line (TDL) or transversal filter
- Variable gain networks (also called taps)
- A summing element
- A controlling mechanism

Some recent equalizers also use one or more TDL for the feedback path, a decision device such as a maximum likelihood decoder, a Viterbi decoder, a slicer, a hard limiters. The detailed schemes are described in detail in Section VII. The function of each component is explained below.

A. Matched Filter

The function of a matched filter can be regarded as equalizing the phase variations introduced in the channel. Forney[4] has combined a matched filter and a transversal filter, calling the combined filter a prewhitened filter. He has shown that the output of a prewhitened filter is a sufficient statistic to estimate the output. This means that there is no loss of information. The matched filter is easily realized by acoustic devices or LSI.

B. Tapped Delay Line

Any equalizer, conventional or adaptive, has a TDL as the principal part. The TDL is used to minimize amplitude variations introduced in the channel. It consists of a number of delay elements. Usually the number is determined by the duration during which the distortion is to be minimized. Each delay element is followed by a variable gain network. The outputs of these taps are time-delayed and attenuated versions of the unequalized input. Addition of the signals gives the equalized output.

The TDL can be realized by either analog or digital components; in practical schemes both types of components have been used. A cable network with RC taps is typical of the analog type, whereas a shift register is a good way of realizing the TDL digitally.

As described above, sometimes an additional TDL is used in a feedback configuration to improve the performance.

C. Control Network

The most important component of any equalizer is the control network. The output of the summing element is compared with either the reference or an estimate of the reference. The difference between the two is usually termed the error signal. This error is used in the control network to set the coefficients of all taps. Thus the function of the control network is to set the taps so as to minimize the error signal.

The coefficient setting of the j^{th} tap at the i^{th} iteration is related to the previous setting by

$$C_j^{(i)} = C_j^{(i-1)} - k\, f(\epsilon_j, x_j),$$

where

$C_j^{(i)}$ = the coefficient of the j^{th} tap at the i^{th} iteration

ϵ_j = the error signal at the j^{th} tap, defined as the ideal signal minus the distorted signal

x_j = the j^{th} signal sample,

and f denotes the function that gives an estimate of the tap distance to be moved as a function of ϵ_j, x_j.

Thus, at any tap the correlation between the error signal and the signal sample is used to set the coefficient. This correlation requires nonlinear components.

The statistically optimum equalizer is nonlinear and is hard to implement. Hence, many people have resorted to suboptimum equalizers, which require only linear elements. It has been stated that "for any criterion of optimality, the optimum linear receiver is expressible as the cascade of a matched filter and a (possibly time-varying) transversal filter."[4] In Section V linear equalizers are dealt with in detail. One example of the nonlinear type is described to indicate the complexity of its elements.

IV Classification of Equalizers

As stated in Section III, the control network needs either the transmitted signal or an estimate of the reference signal. Frequently, the reference signal is not available at the receiver. In some cases, the tap settings are done by transmitting predetermined test pulses. These pulses are exactly known at the receiver, when the tap settings have been done, they are frozen. Hence, such an equalizer is called fixed or automatic.[2] Since the channel is dynamically changing, fixed tap settings will not equalize the channel under all conditions.[3] Therefore, to make the equalizer adapt to the channel variations, the transmitted signal is used as reference in the control network. On the basis of these methods of setting the taps, equalizers are divided broadly into automatic and adaptive types. There are also variations of the adaptive equalizers, such as decision feedback and adaptive decision feedback.

A second classification is based on the nature of the control network. With this as the basis, equalizers are classified into linear and nonlinear.[20]

A third classification is based on the error that is optimized. If this error is absolute, the zero forcing (ZF) equalizer results. The mean-square equalizer, as the name implies, minimizes the mean-square error. The scheme based on the maximum likelihood decision rule results in the max-likelihood equalizer.

The adaptive feature can be introduced into any of these schemes. The mean-square type of equalizer with adaptive feature has been used in many practical situations.

V Description of Typical Schemes

A. Zero Forcing (ZF)

As the name indicates, the ZF equalizer forces zeros into the channel impulse response, at desired places. Figure 3 illustrates a typical equalizer based on this principle.

The amount by which the j^{th} tap is to be moved is given by the relation

$$\hat{h}_j = \Sigma \operatorname{sgn}(e_j) \operatorname{sgn}(y_{i-j}), \qquad (2)$$

where

$\hat{h}_j$ = the estimate of h_j, the amount by which the j^{th} tap is to be moved

e_j = the error signal at the j^{th} tap

y_j = the j^{th} sample of equalized output and sgn denotes the signum function.

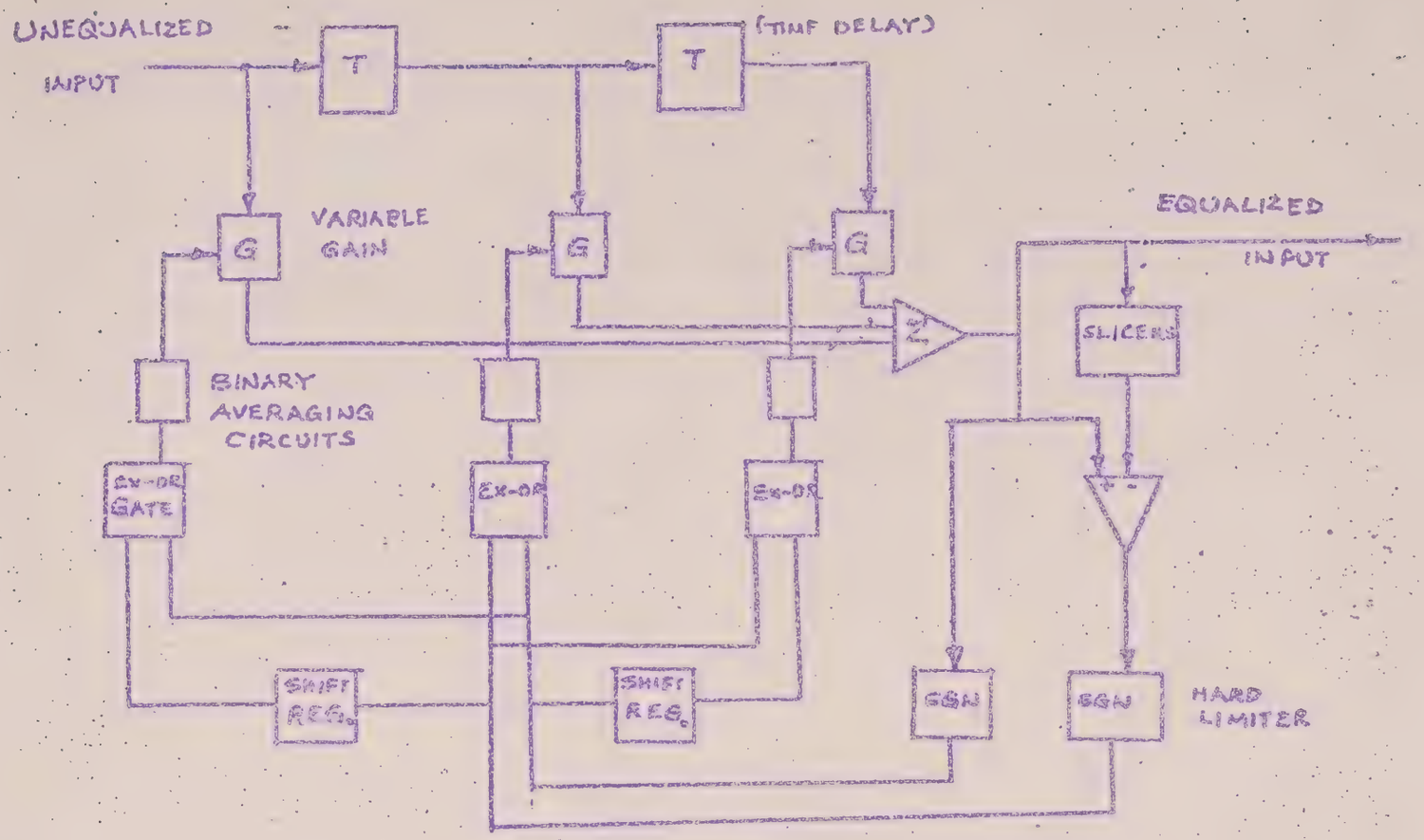


FIG 3. IMPLEMENTATION OF EF ALGORITHM

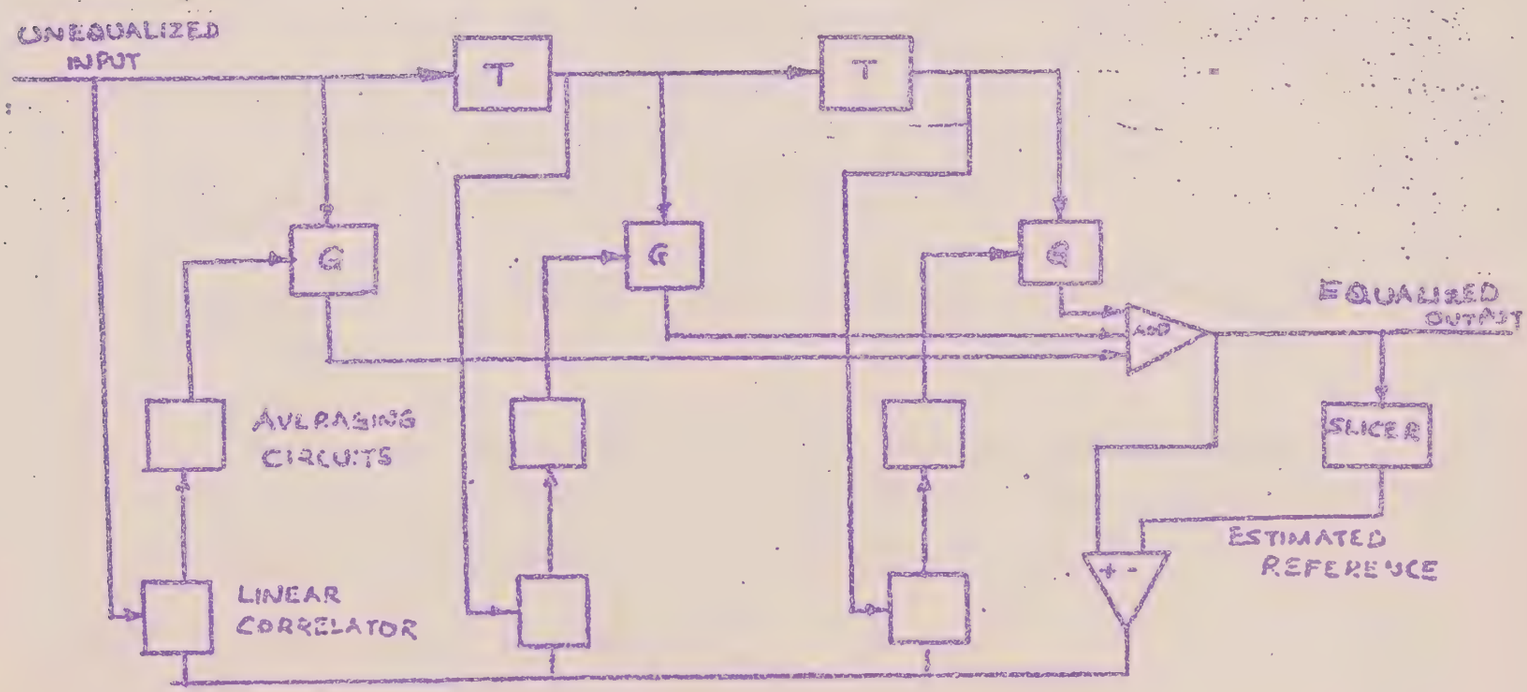


FIG 4. CIRCUIT FOR MEAN-SQUARE ALGORITHM

The error signal e and the equalized output y are passed through hard limitors that form signum functions. These functions are time-delayed relative to one another by shift registers, before binary multiplication. The resulting signal is binary averaged and used to set the taps, as shown in Eq. (2) and Figure 3.

It can easily be shown[6] that the above tap settings minimize the peak distortion D_{peak} given by

$$D_{peak} = \sum_{i \neq o} (h_i),$$

where h_i is as described in Eq. (2).

Thus, the above scheme requires binary elements such as shift registers and exclusive or gates. The adaptive feature can easily be introduced into this. Such schemes usually take a long time to reach steady state because the convergence rate is low.

If in the above scheme the unequalized input, instead of the equalized output, is correlated with the error signal, a modified zero-forcing (MZF) scheme results. It can easily be seen that the hardware requirements for the two schemes are the same. But MZF has better convergence properties. In this case,

$$\hat{h}_j = \Sigma \text{ sgn } (e_i) \text{ sgn } (X_{i-j}), \tag{4}$$

where $\hat{h}_j$ and e_i are defined by Eq. (2), and X_i is the i^{th} unequalized input sample.

Another variation of ZF, which has still better convergence properties, can be obtained[6] by clipping the error signal alone. In this case, the relationship can be written as

$$\hat{h}_j = \Sigma \text{ sgn } (e_j) \, X_{i-j}. \tag{5}$$

This scheme is referred to in the literature as a hybrid equalizer.

B. Mean Square Equalizer:MSE

In contrast to the above schemes, here the mean-square error is minimized. The amount by which the j^{th} tap is to be moved is given by

$$\hat{h}_j = \Sigma\, e_i\, X_{i-j} \qquad (6)$$

where e_i, X_i are as defined by Eqs. (2), (4), and (5). The estimate $\hat{h}_j$ is obtained by linear correlation of the error and a delayed version of the unequalized input..

The above algorithm can be implemented as shown in Figure 4. As can be seen from that figure, this requires a linear correlator or a multiplier and summer, and hence the circuitry is complex. But this algorithm has been shown[6] to have excellent convergence properties, and it minimizes the mean square error given by

$$D_{ms} = \sum_{i \neq o} h_i^2 . \qquad (7)$$

It has been shown in the literature[6] that the MSE and Hybrid types converge to almost the same value, although the rates of convergence are different. Figure 5 compares the four schemes with regards to the convergence rate.[6]

C. Discrete Kalman-Type Equalizer

This method uses a discrete version of Bellman's dynamic programming. The general scheme, as shown in Figure 6, is linear and hence statistically not optimum. The quasi-linearization method is used to incorporate the adaptive feature. This type of equalizer[5] is superior to others only if the channel behavior is known in advance.

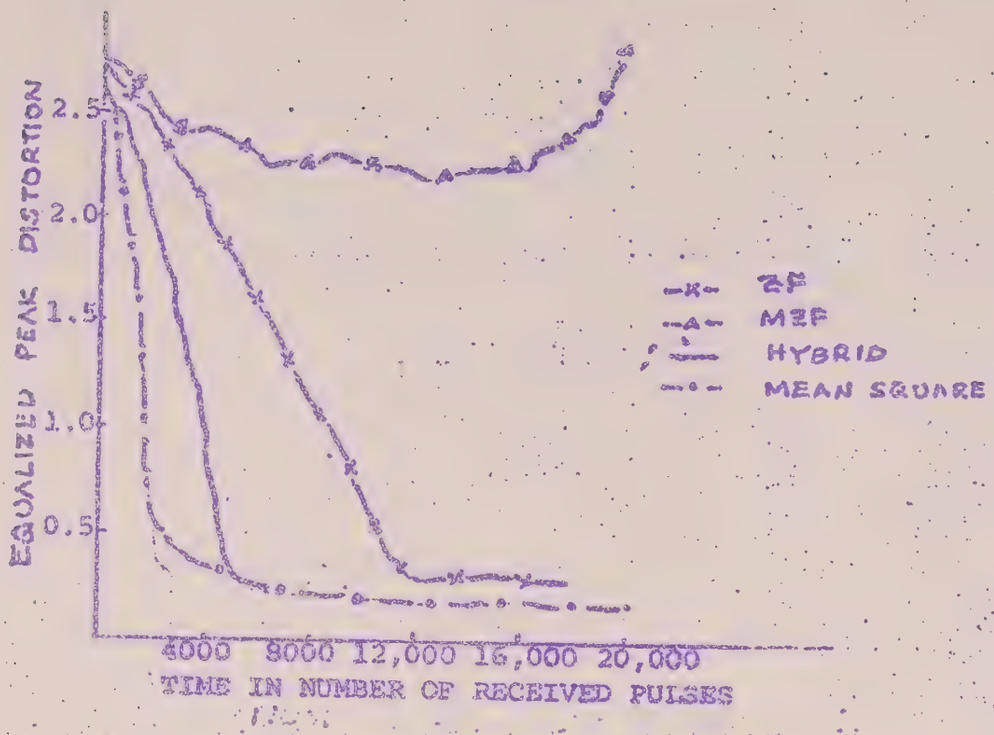


FIG 5. A COMPARISON OF VARIOUS LINEAR EQUALIZERS
(By computer simulation: from Ref. 6)

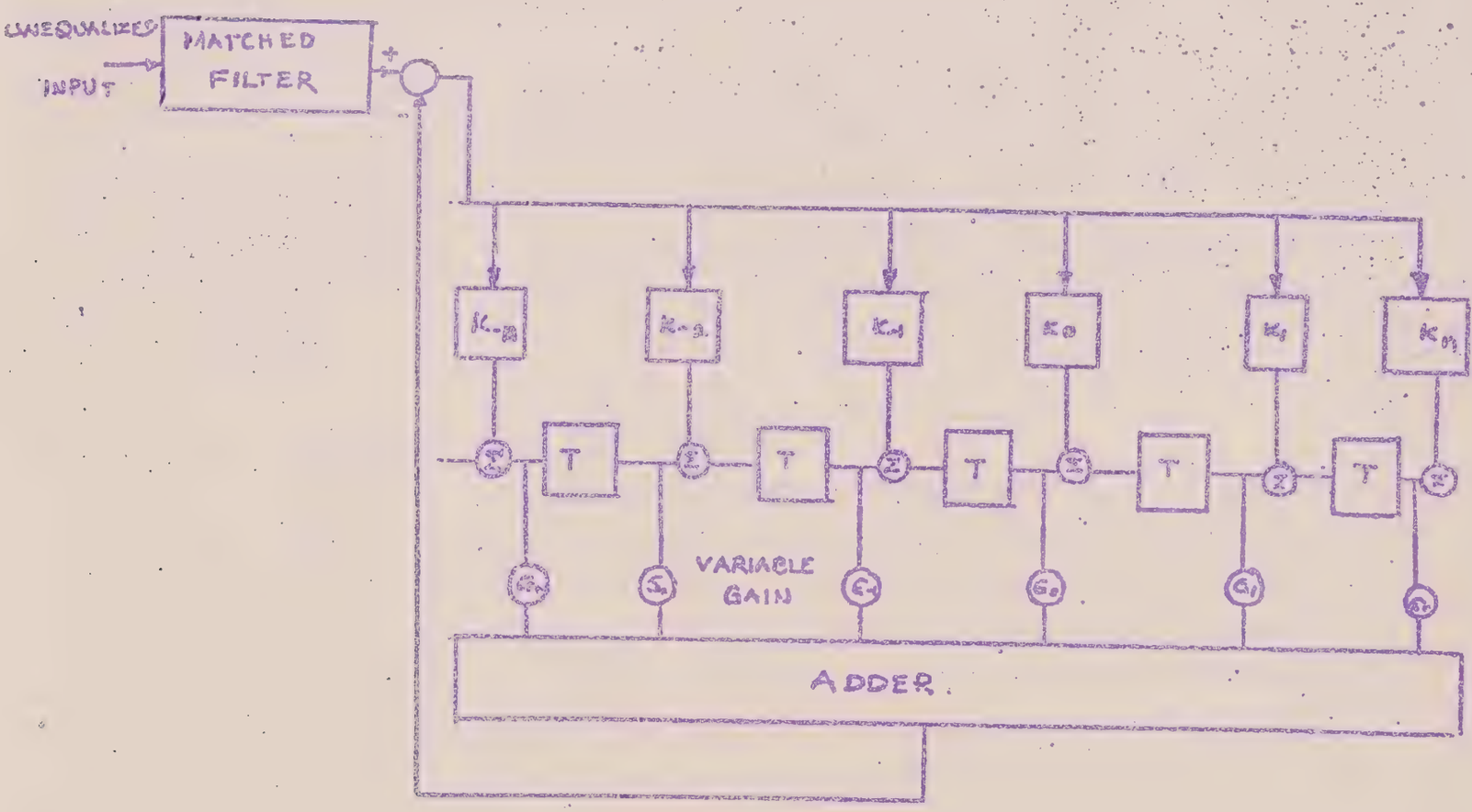


FIG 6. KALMAN FILTER EQUALIZER

D. Maximum Likelihood (ML) Equalizer

The ML criterion results in a nonlinear equalizer. Here the equalization problem is regarded as an estimation problem. If the equalizer uses a Viterbi decoder for estimating the input, the resulting scheme is shown to have less bit error rate. Such an equalizer essentially consists of a prewhitened filter (a cascade of a matched filter and a transversal filter), a sampler, and a Viterbi decoder. No feedback is used. This scheme has been analyzed for partial response class IV systems using telephone channels and has been successfully implemented.[3]

An entirely different version of equalizer in which a Viterbi decoder is used in the feedback path was described recently. Here the function of the Viterbi decoder is to estimate the transmitted signal as closely as possible, to compre it with the equalized output. The hardware requirements of the Viterbi decoder are memory circuits and logic. This scheme is shown in Figure 7.

The basic idea here is to choose the survivor at each sampling instant among all possible paths. The complexity of a Viterbi decoder can be expressed in terms of input alphabet m, and the amount of inter-symbol interference to be handled is expressed in bit lengths (L). Such a decoder requires m^L additions, m^{L-1} storage spaces, and m^L (m-1) comparisons.

VI Decision Feedback Equalizer (DFE)

This is a fixed type of equalizer; the schematic diagram is shown in Figure 8. Two TDLs are required, one in the forward path and the other in the feedback path. This type of equalizer is known[8] to have good convergence properties. The basic assumption here is that the past decisions are correct, and hence these decisions are used to eliminate the distortion caused by past digits. The residual distortion after equalization is mainly due to future digits. The implementation is not

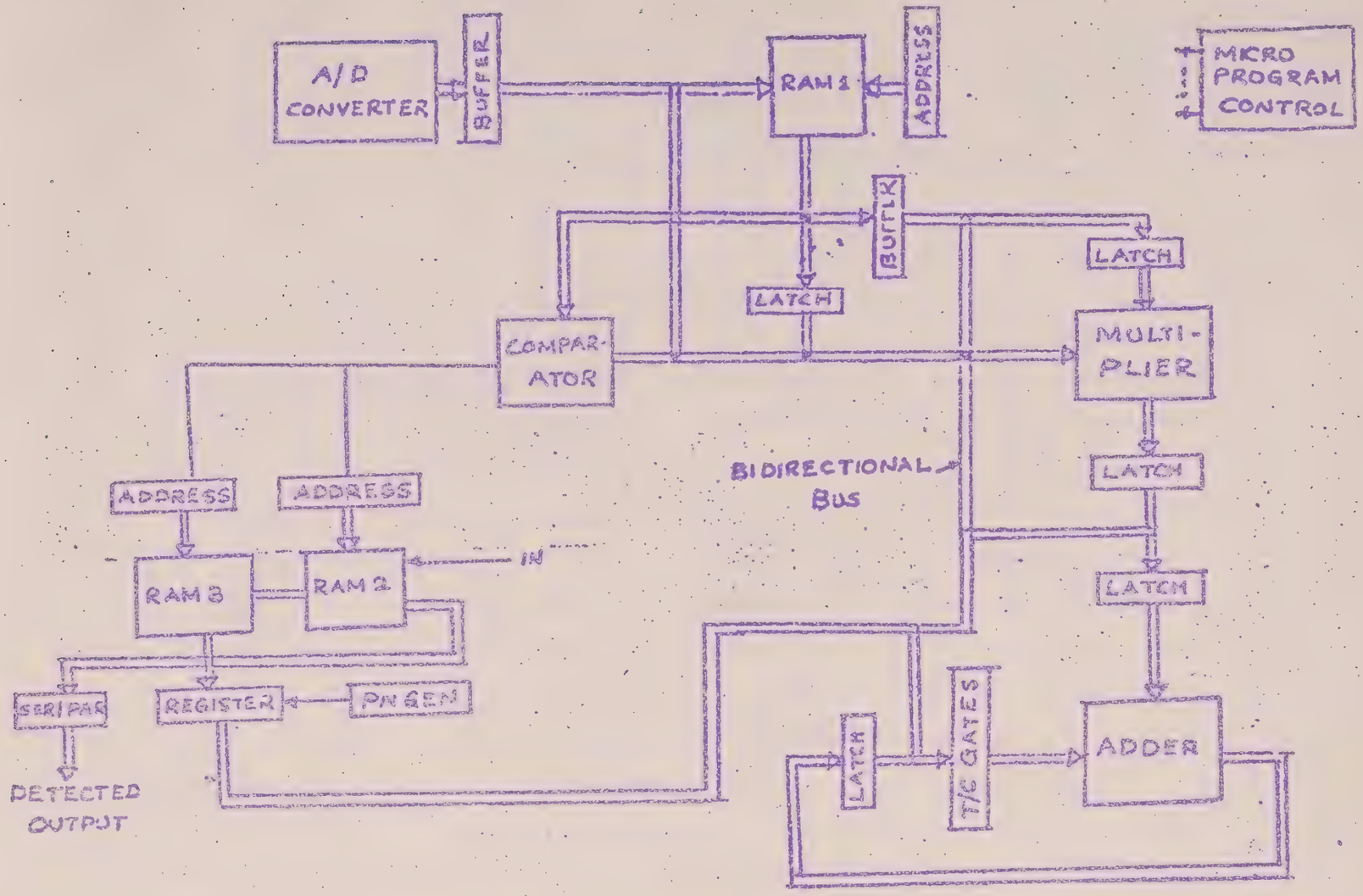


FIG 7. BLOCK DIAGRAM OF POSSIBLE IMPLEMENTATION OF VITERBI DECODER.

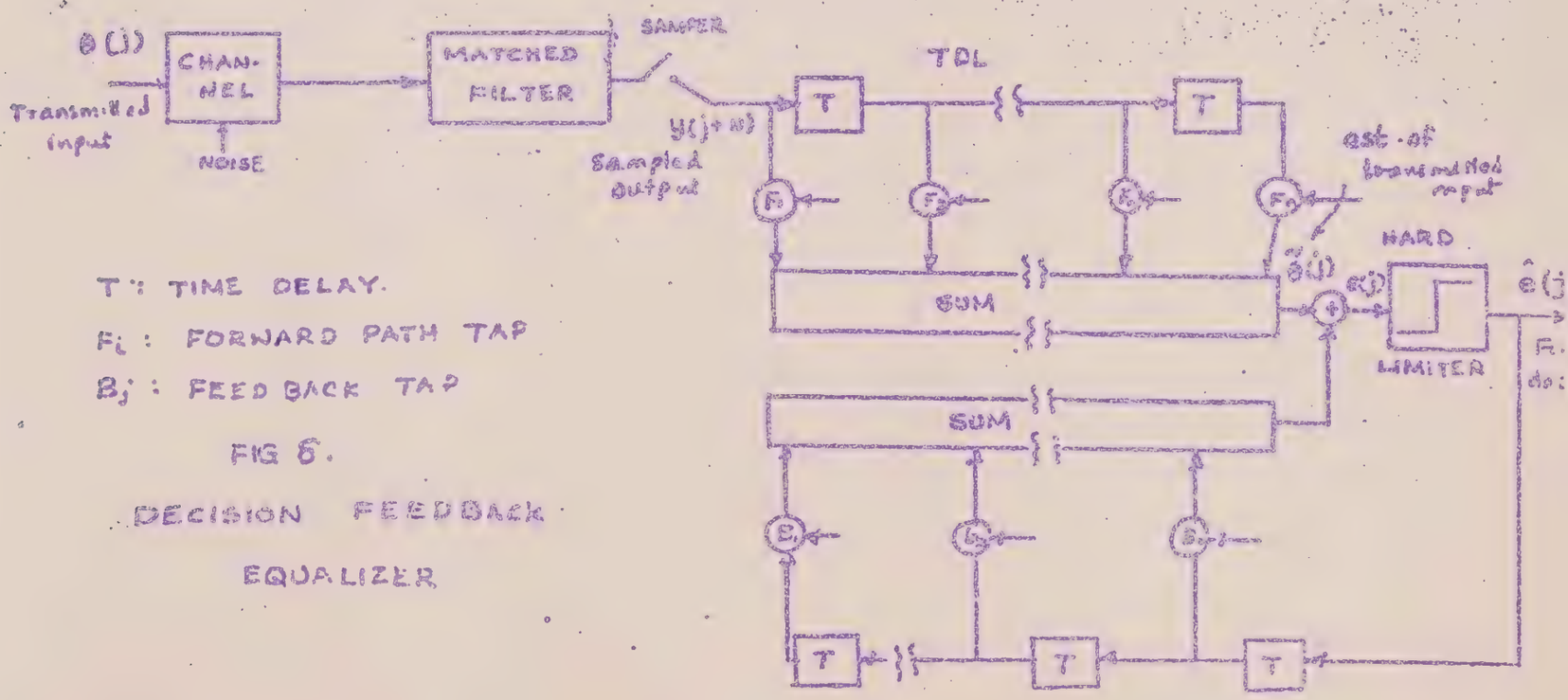


FIG 8.

DECISION FEEDBACK EQUALIZER

very difficult, but it requires predetermined test pulses. The performance is shown to be very good if the channel variations do not fluctuate too much.

A. Adaptive Decision Feedback Equalizer (ADFE)

The DFE is a fixed type. To make the equalizer useful in situations where channel variations vary widely, an adaptive feature is introduced into the DFE. There are several ways to implement adaptive features. One of the schemes uses the correlation between $\hat{e}_{(j)}$ and $y_{(j+k)}$ to set the forward taps and correlation between $\hat{e}_j$ and $\hat{\theta}_{j-m}$ to set the feedback taps. As shown in Figure 8, $\hat{e}_{(j)}$ is the error between the output of the first tapped delay line and the output of the feedback loop which includes a second tapped delay line. The unequalized received signal is $y_{(k)}$ and $\hat{\theta}_{(j)}$ is the equalizer output. This scheme sets the taps very near to optimum values. Also, it can easily be shown that the mean-square error is a quadratic function of the tap values.

Since the MSE is a quadratic function of the tap settings, several algorithms, such as steepest descent, conjugate gradient, and gradient projection, have been used to improve the convergence. Some of the algorithms are faster than others, but the gradient projection method is shown to converge in L steps, where L is the number of taps used in the scheme.

Other schemes have been mentioned, but these are only modifications of the above schemes. Equalizers have also been analyzed in the frequency domain.

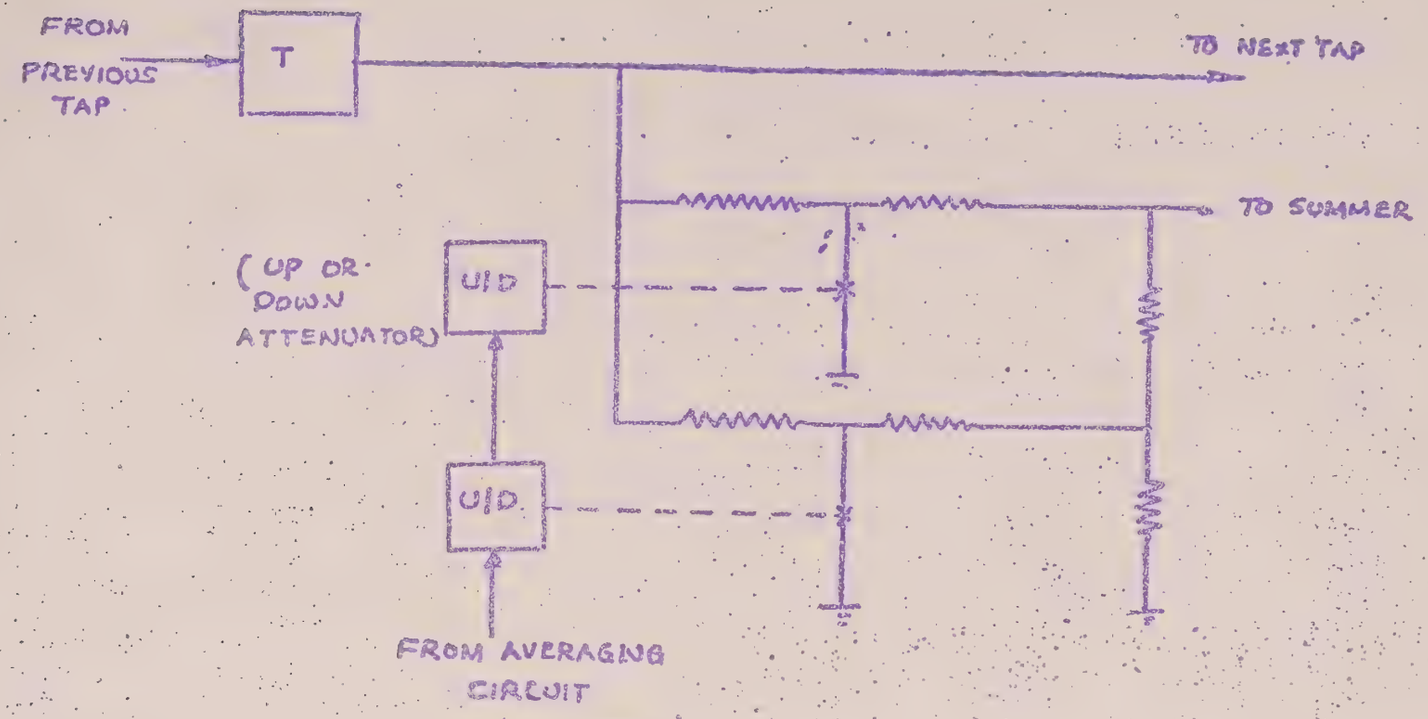
VII Hardware Realizations

As described earlier, several equalizers have been built for telephone and television. These schemes have been summarized in Table 2, with the method of realization of each component. The convergence rates and complexity of the schemes are compared to indicate the relative merits.

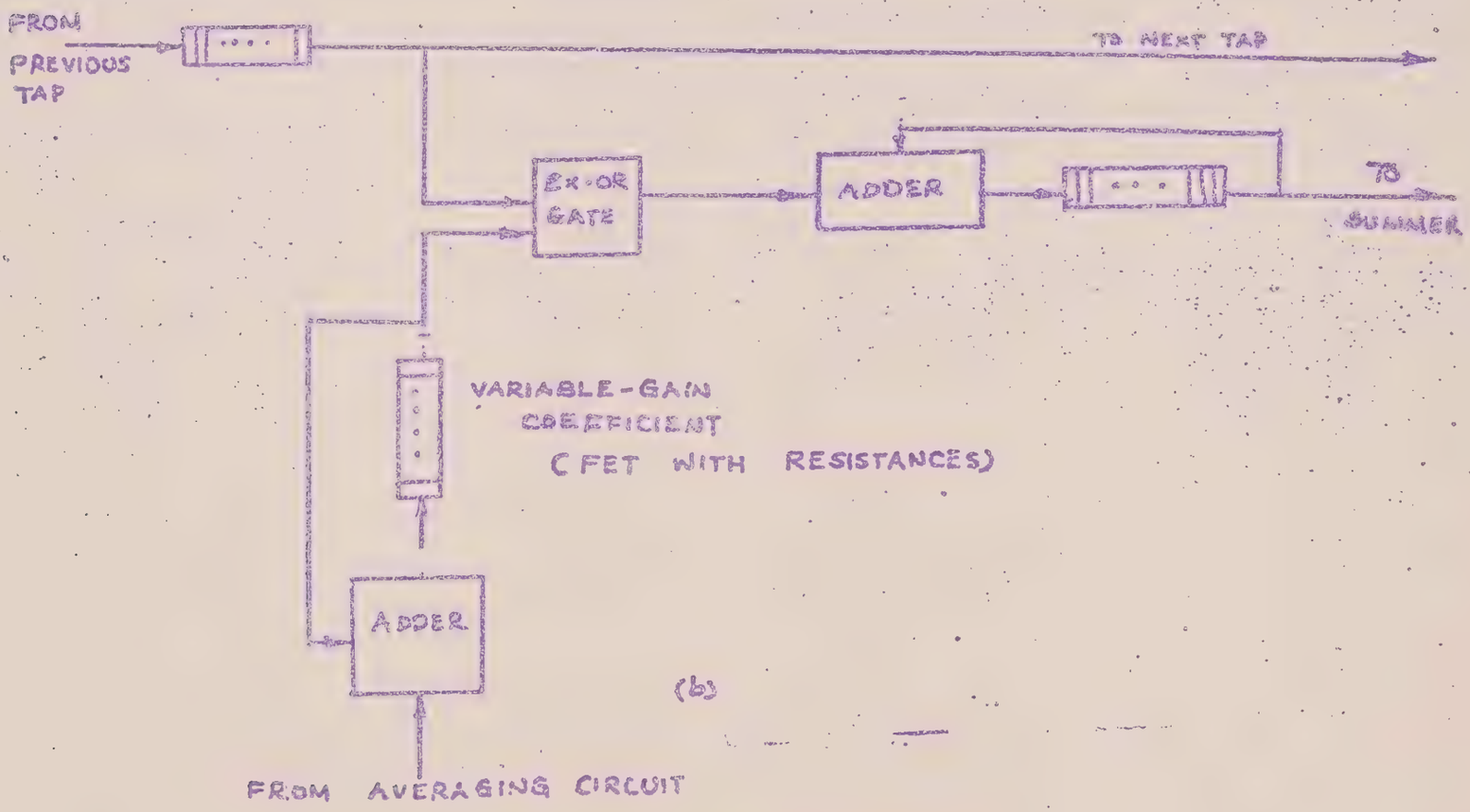
Table 2

SUMMARY OF EQUALIZER SCHEMES--WITH HARDWARE

Principle or Type	Description	Reference	Use	Remarks
Z/F/NZF, fixed adaptive, analog, semidigital	Shift register (TDL), binary correlators, binary averaging circuits, variable-gain circuits, operational amplifier, hard limiter, slicer	Figs. 3, 9 (a) Ref. 6	Telephone	Easy to implement, not complex; harge size; convergence very slow
MS, fixed/adaptive, digital	Shift register F/F (TDL), X-OR gates, adders, variable gain circuits, slicer, hard limiter	Figs. 4, 9 (b) Ref. 6	Telephone	Cost high; convergence better than above; medium size; complex
Decision/feedback, fixed/adaptive, digital, MS	A/D conversion, shift register, linear correlators, adders, storage devices (F/F), X-OR, transistor switch, error sensing and decoding network, accumulator realization by full adders	Fig. 10(a), (b) Ref. 11	Telephone (data)	Convergence medium; can be adaptive; not very complex; large size
Nonlinear, MS, adaptive	Shift register, soft limiters, adders, decision elements, (transistor, register, diode, optional amplifiers); see Fig. 11(b)	Fig. 11(a), (b) Ref. 12	Telephone (data)	Very complex; no feedback; very good performance; medium size; good convergence
Maximum likelihood, fixed, digital	Prewhitened filter (matched filter in cascade with TDL) sampler, Viterbi decoder (memory, adders, comparators)	Fig. 7 Refs. 4,7	Telephone (data)	Excellent performance; complex circuitry; large size; convergence no problem; low BER
ZF, analog, adaptive, no feedback	Delay line (cable circuit) digitally controlled attenuator, solid-state linear switches, summing and clamping circuits, timing CKTS, comparators	Ref. 10	Television	Size too great; moderate performance; mostly analog components; cost high; convergence slow



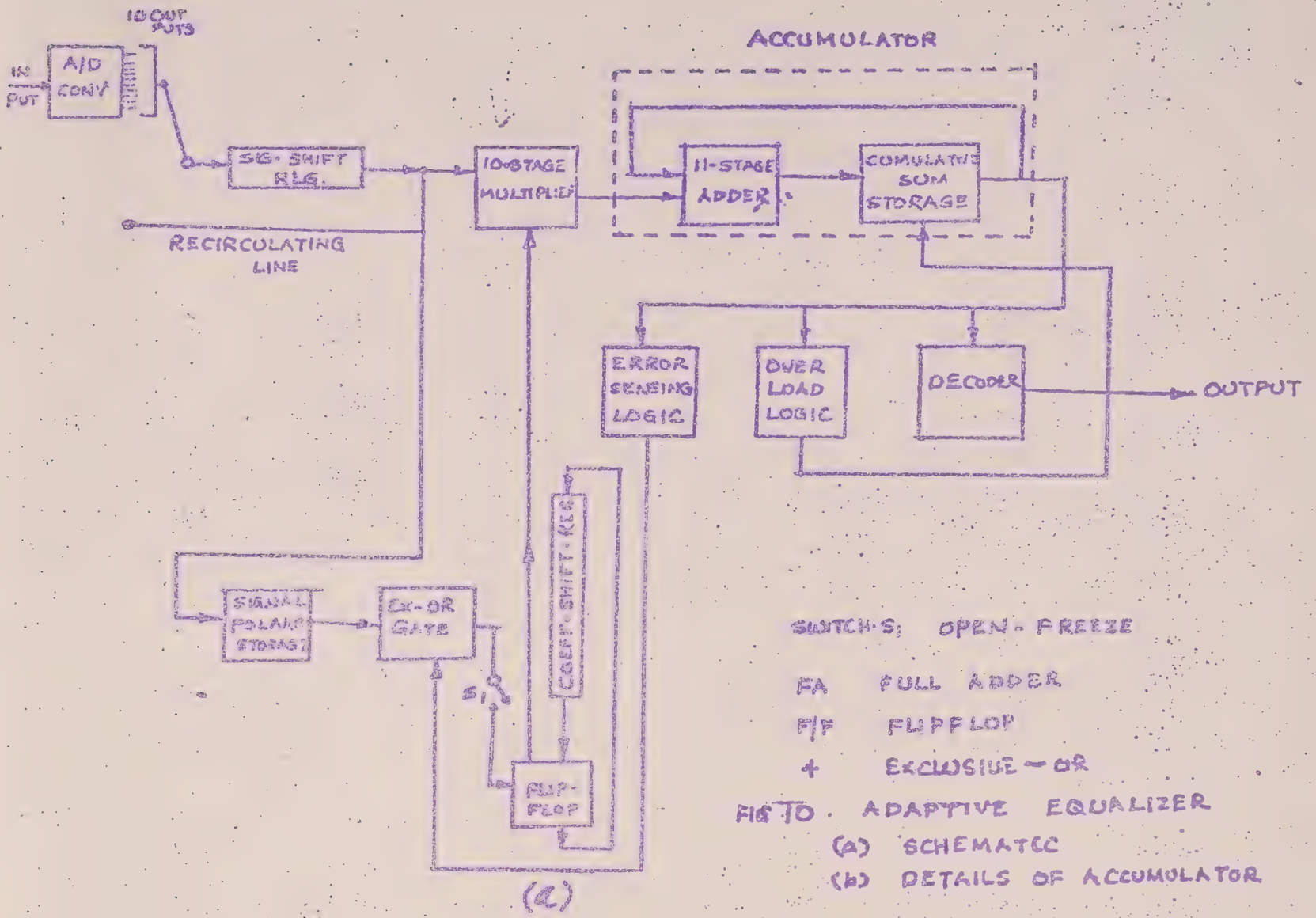
(a)

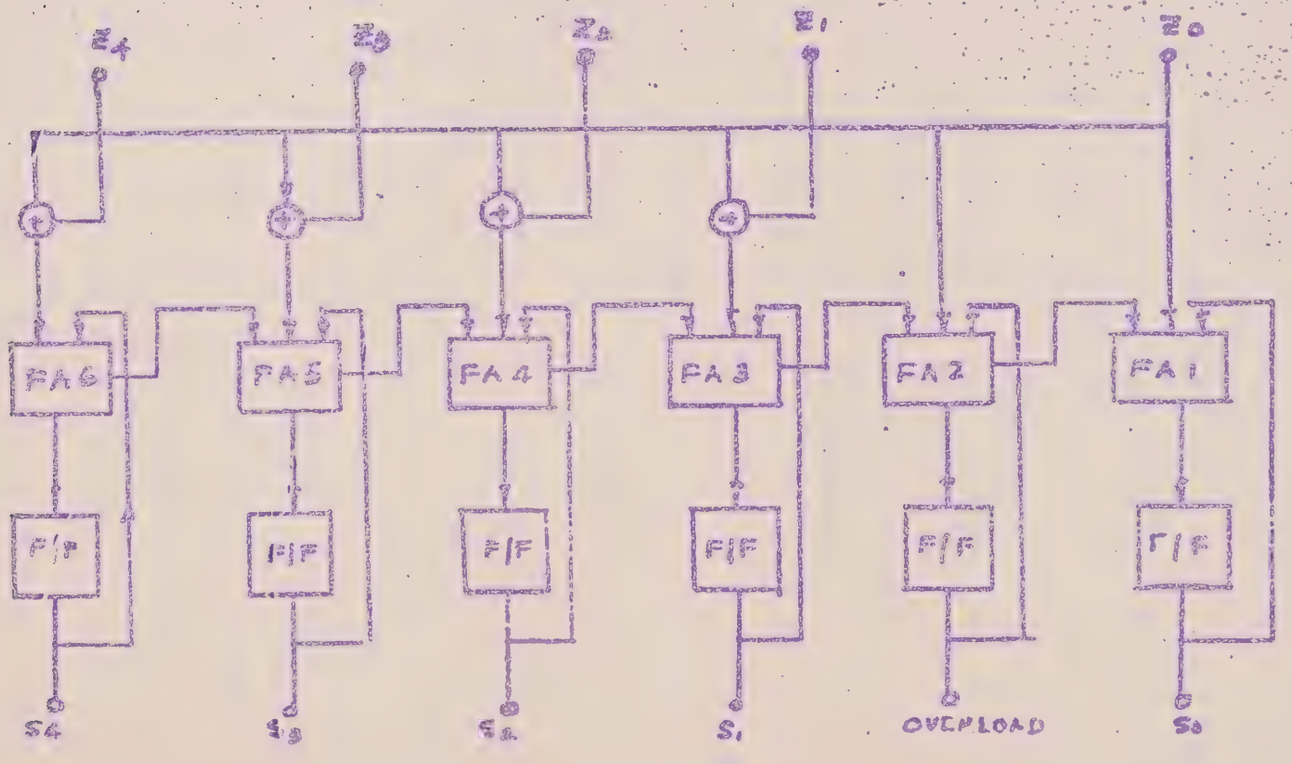


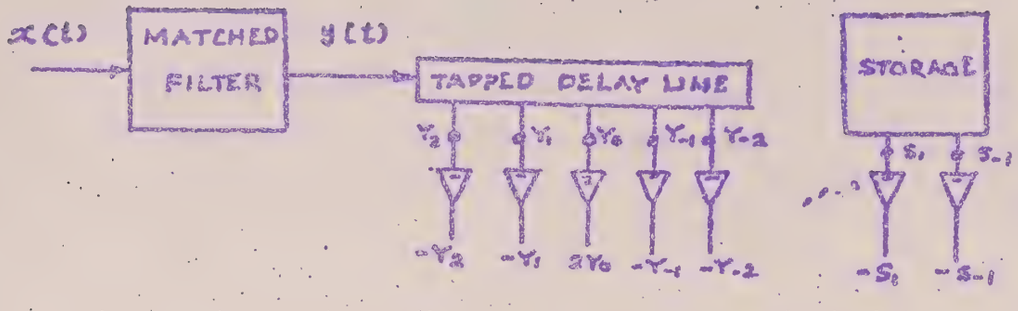
(b)

FIG 9 a) SEMI DIGITAL IMPLEMENTATION

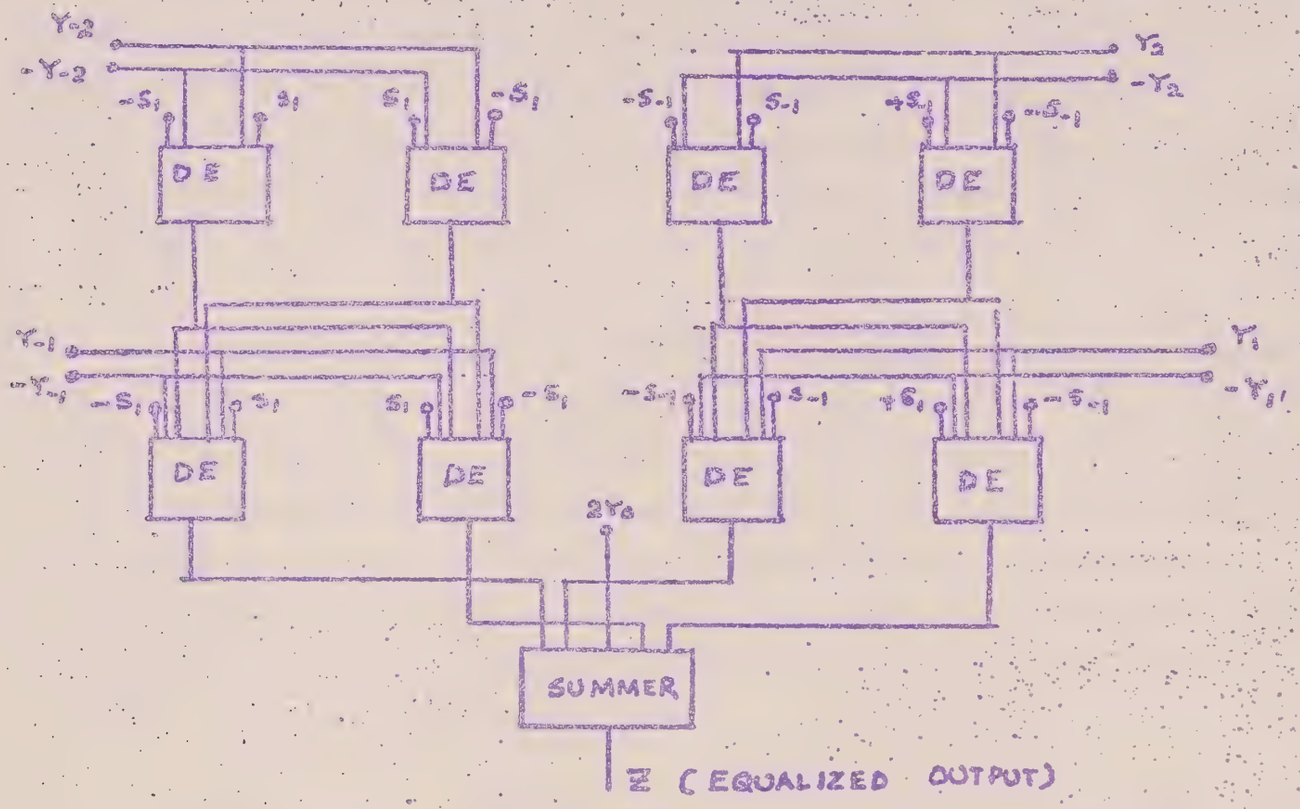
b) DIGITAL IMPLEMENTATION PER TAP CIRCUITRY


10 OUTPUTS
INPUT
A/D CONV
SIG. SHIFT REG.
10-STAGE MULTIPLIER
ACCUMULATOR
11-STAGE ADDER
CUMULATIVE SUM STORAGE
RECIRCULATING LINE
ERROR SENSING LOGIC
OVER LOAD LOGIC
DECODER
OUTPUT
SIGNAL POLARITY STORAGE
EX-OR GATE
COEFF. SHIFT REG.
S1
FLIP-FLOP
(a)
SWITCH S1 OPEN - FREEZE
FA FULL ADDER
F/F FLIPFLOP
+ EXCLUSIVE - OR
FIG 10. ADAPTIVE EQUALIZER
(a) SCHEMATIC
(b) DETAILS OF ACCUMULATOR

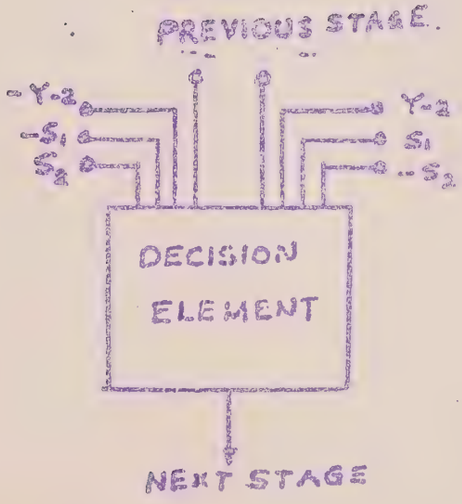

Z6
Z5
Z4
Z3
Z2
Z1
Z0
FA6
FA5
FA4
FA3
FA2
FA1
F/F
S4
S3
S2
S1
OVERLOAD
S0
(b)

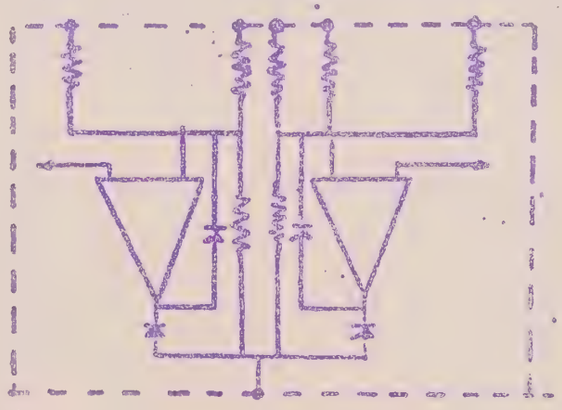


(c)



(a)





(b)

FIG: 11 NONLINEAR EQUALIZER (a) SCHEMATIC (b) DETAILS OF DECISION ELEMENT

VIII Performance of Equalizer

The quality of an equalizer is based on the following factors: stability, error propagation, enhancement of noise, adaptation time, residual steady-state error, step size of taps, bit error rate, and economy.

The stability deals with the capability of the equalizer to maintain tapesettings in the presence of output errors. The error propagation is caused because the past decisions are used to decode present outputs. Some of the equalizers although reducing intersymbol interference by zero-forcing or tailcutting increase the noise level in the receiver. This is usually referred to as noise enhancement. It has been shown that the DFE equalizer is more prone to enhance noise than a conventional equalizer.

Adaptation time and residual error can be explained with reference to Figure 12. Here the mean-square error is plotted as a function of time. The adaptation time is defined as the time taken for the equalizer to reach steady-state error. This time is a function of the convergence rate and the step size. The steady-state error is the residual error when the equalizer has reached steady-state conditions. This error is lower bounded below by the performance of a one shot receiver when there is no intersymbol interference.

The bit error rate is shown to depend on the signal-to-noise ratio. The relationship of the bit error rate and the signal-to-noise ratio is shown in Figure 13. This figure is reproduced from the simulation results given in Ref. 7.

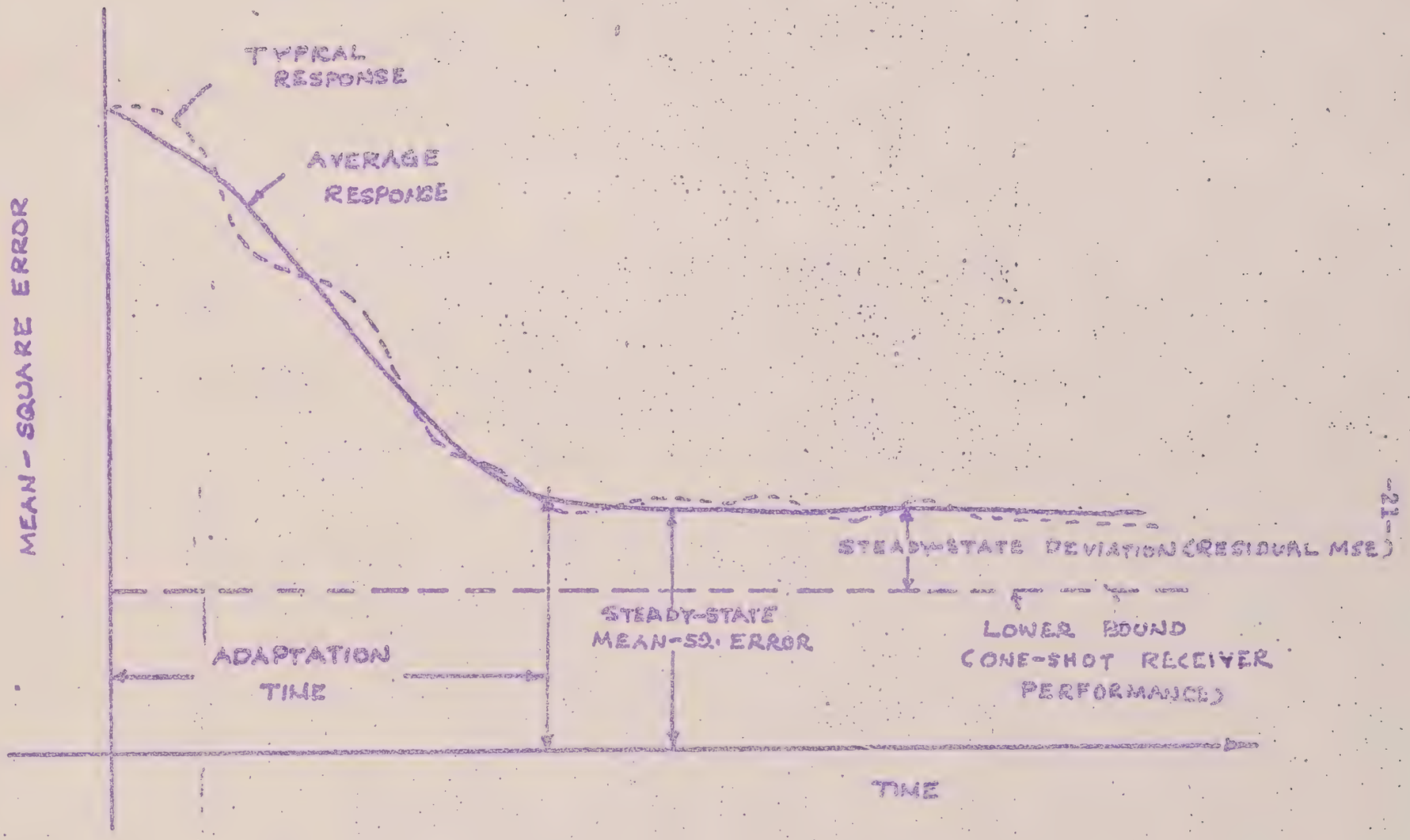


FIG 12 GRAPH SHOWING MEAN-SQUARE ERROR AS A FUNCTION OF TIME

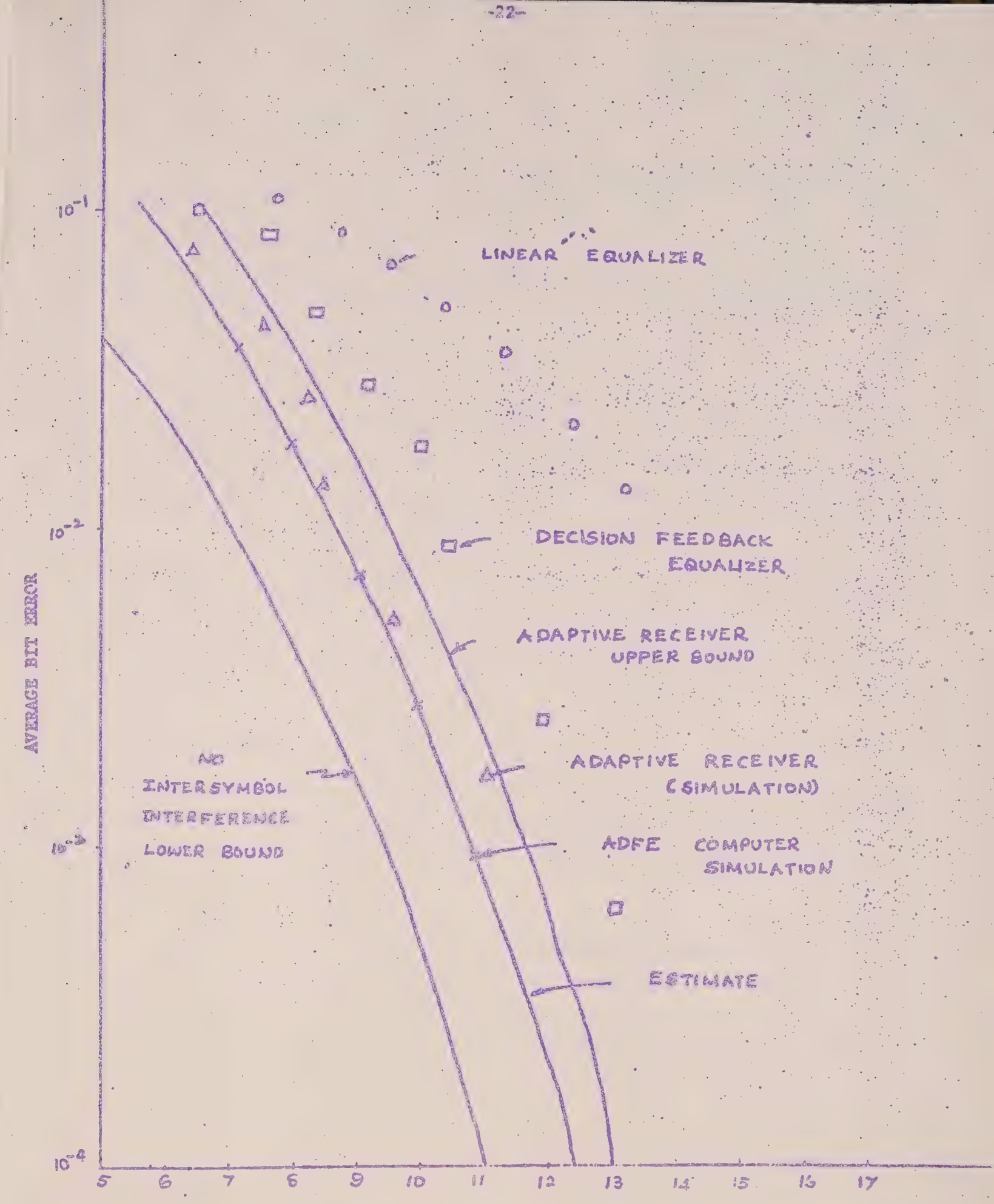


FIG 13. AVERAGE BIT-ERROR PROBABILITY AGAINST OUTPUT SNR

(TAKEN FROM REF. 7)

IX Evaluation of Equalizers

Equalizers are evaluated[14] on the basis of such performance factors as adaptation time, bit error rate, complexity, economy, and size. The evaluation is typically done with the equalizers under identical conditions. These conditions are simulated either by hardware or by computer. To compare various schemes, computer simulation usually seems to be best.

A typical comparison between the conventional and adaptive feedback equalizers is described below. For a channel with a 100-MHz bandwidth at -3.0-dB points, a 240-MHz bandwidth at -20.0-dB points, and a 70.0-dB-per-octave roll-off at the higher frequencies, the data rates were 225 Mb/s without equalization, 400 Mb/s with a linear equalizer, and 450 Mb/s with a decision feedback equalizer. A DFE with 21 forward taps could not perform equalization, whereas a decision-feedback equalizer with five forward taps and six feedback taps did very well with the same channel. The above results show that the ADFE outperformed the linear equalizer.

X Packet Radio Issues

The description given above is general and applicable to any situation. Below, the issues are reviewed in detail to explore the possibility of use of equalizers. In TPRW 28, Fralick indicated that equalizers could improve the performance of PRN.

Since the typical channel characteristics are not known precisely at present, the results available for similar channels are used below to explain the details. Turin's[22] measurements have shown that the delay spread varies between 5 and 10 μs. Assuming the worst case, the delay spread is taken as 10 μs.

The data rate for PR is assumed to be 100 kb/s, which gives a bit period of 10 μs. To calculate the delay time of a TDL, either the bit rate criterion or a sampling theorem is used. If the bandwidth is used efficiently, the criteria should give the same values. Otherwise, the lesser of the two is taken. The bandwidth assumed is 40 MHz:

$$\text{Delay time} \quad \begin{cases} \text{Using bit rate} = 10\ \mu s. \\ \text{Using sampling theorem} = \dfrac{1}{2 \times 40} \times 10^{6} = 0.0125\ \mu s. \end{cases}$$

Clearly, the bandwidth is not efficiently used. If the sampling theorem criterion is used, the equalizer requires $\frac{10}{0.0125} = 800$ taps, which is very unrealistic. If the bit-rate criterion is used, the equalizer requires one tap, which is trivial. Hence if the 100-kb/s rate is used, it is clear that there is no need to use an equalizer, provided the 10-μs. characteristic is satisfied by the PR channel.

To explain the complexity involved and other issues, such as typical hardware required, two hypothetical situations are analyzed below. The first situation is almost the same as PRN, but the bandwidth is used more efficiently, and the spread to be covered is modified. The parameters are:

$$\begin{aligned} \text{Bit rate} &= 100\ \text{kb/s} \\ \text{Bandwidth} &= 60\ \text{kHz} \\ \text{Spread to be covered} &= 100\ \mu s. \\ \text{Delay required} &= \begin{matrix} 10\ \mu s.\ \text{(bit rate criterion)} \\ 8.25\ \mu s.\ \text{(sampling theorem)} \end{matrix} \\ \text{Minimum delay} &= 8.25\ \mu s. \\ \text{Number of taps} &= \frac{100}{8.25} = 12 \end{aligned}$$

If the conventional linear equalizer is used, all the 12 taps are located in the forward path. But if the ADFE is used, the taps are distributed with five in the forward path and seven in the feedback path. Generally, the number of feedback taps is greater than the number of forward-path taps. This is to subtract the effect of past decisions as much as possible.

For the above scheme (assuming ADFE), the hardware requirements are:

Sampler with a rate of 120 k/s

Storage = 12 bits for TDLs

Multiplications/second: 12 parallel multipliers each with a rate of 120 k/s

Summing element with 8.25 -s.

Variable gain networks.

If the Viterbi decoder is used, in addition to the above, the following are required:

2^{12} addition circuits

2^{11} storage spaces

2^{12} binary comparison circuits.

Hard limiters and slicers.

The parameters for the second situation are:

Bit rate = 1 mb/s

Bandwidth = 500 kHz

Spread to be covered = 10 μs. (as given by Turin's paper)

Here also the bandwidth is efficiently used.

Delay required = 1 μs. (bit-rate criterion)
1 μs. (sampling theorem)

Minimum delay = 1 μs.

Number of taps = 10.

In the conventional equalizer all the ten taps are in the forward path. But, if the ADFE is to be used, the taps can be distributed either equally between the forward and feedback paths or four in the forward path and six in the feedback path. The second distribution results in better preformance, since more effect of past decisions is substracted in the feedback path.

The hardware necessary for this scheme is:

Sampler with a rate of 1 m/s

Storage = 10 bits for TDL

* Multiplications/second: 10 parallel multipliers each with operating time of 1 μs.

Summing element with 1 μs.

Variable gain networks and hard limiters

In case a Viterbi decoder is used, additional hardware is required:

2^{10} adding circuits

2^{9} storage spaces and 2^{10} binary comparators.

The typical times required are of the order of μs. Hence reliable, economical precise components are to be chosen for delays, storages, taps, multipliers, and adders. This suggests the use of LSI. Little can be said about these firmly, since no equalizer at this time is built of LSI components.

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* Recently Texas Instruments developed a multiplier chip which takes 17 nanosecs for 16 bit multiplication. Hence this multiplication seems practical and feasible.

The following factors are of prime importance for PR with regard to equalizers:

- Bit error rate
- Size
- Economy.

The bit error rates should be of the order of 10^{-6}. This mainly dependent on signal-to-noise ratio. The size poses severe limitations if the equalizer is to be located in the terminal. The main competitors are regards the size are LSI and SAWD's. But little can be said since SAWD's are still in the developing stage. The final decision is to be based on the economics of equalizers.

The above paragraphs can be summarized. With present data rates and bandwidth, there is no real need for equalizers. But the final decision can be made when the following characteristics have been more precisely defined.

(1) Bit rate
(2) Bandwidth to be used
(3) Location of equalizer
(4) Type of modulation
(5) Interference length to be covered
(6) Economics.

Items (1), (2), and (5) determine the exact number of taps. Item (3) poses size problems, and hence determines the type of components to be chosen. Knowledge of Item (4) is required to answer such questions as the necessity of a matched filter and the need for an equalizer, since it is shown that some of the modulation schemes will not be improved by equalization. Finally, the economics are to be kept in mind to decide the feasibility for PR.

XI Conclusion

The problem of equalization has been described in detail. The typical components required in an equalizer have been illustrated functionally. The several existing schemes have been detailed to compare their merits and complexity. Existing technology cannot be extended simply, because of the wide differences in requirements for PR. The hardware possibilities are LSI and SAWD's, if the size of the equalizers are to be small. The PR issues have been explained. Since the exact characteristics are not precisely well defined, two hypothetical cases similar to PR have been analyzed in detail to illustrate the requirements of typical equalizers. The final decision can be made only if the characteristics are known better. The equalizers will be further investigated in regard to economics and location when the characteristics have become well known.

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